								Page 1 of 3				
			 		ATTY, DOCKET NO. 1875.138000F	APPLICATION NO. (to be assigned)						
FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT					APPLICANTS Ralph Duncan et al.							
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INITIAL		DOCUMENT NUMBER		DATE	NAME	CLASS	SUB-CLASS	FILING DATE				
2	AA1	4,211,9	975	07/1980	Kuroda -	-						
8	AB1	4,789,9	976	12/1988	Fujishima							
0	AC1	4,818,9	903	04/1989	Kawano							
0	AD1	4,903,	329	02/1990	Marik et al.							
P	AE1	5,031,		07/1991	Ragan							
19	AF1	5,200,		04/1993	Seong	-						
R	AG1	5,311,		05/1994	Dobrovolny							
19	AH1	5,329,		07/1994	Chan et al.							
100	 	1			Taketoshi et el.							
0-	Al1	5,389,		02/1995								
	AJ1	5,423,		06/1995	Westergren et al.							
0	AK1_	5,428,	829	06/1995	Osburn et al.							
	,		·	· FOREIGI	N PATENT DOCUMENTS	T	T					
EXAMINER INITIAL		DOCUMENT NUMBER		DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION				
8	AL1	37 23	778 A1	01/1988	DE	H03L	7/10	Yes X No				
0	AM1	195 06	324 C1	10/1995	DE	нозн	21/00	Yes X No				
0	AN1	0 393	717 A2 & A3	10/1990	EP	нозн	11/12	Yes No				
0	AO1	0 431	887 A2 & A3	06/1991	EP	H03L	1/02	Yes No				
0	AP1	0 535	536 A1	04/1993	EP	H01L	27/02	Yes No				
		1		OTHER (Including Au	thor, Title, Date, Pertinent Pages, etc.)							
8	AR	Burghartz, J. N. et al., "High-Q Inductors in Standard Silicon Interconnect Technology and its Application to an Integrated RF Power Amplifier," International Electron Devices Meeting Technical Digest, IEEE, pp. 1015-1017 (December 10-13, 1995).										
2	AS	1	Craninckx, J. and Steyaert, M.S., *A 1.8-Ghz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors,* <i>IEEE Journal of Solid-State Circuits</i> , Vol. 32, No. 5, IEEE, pp. 736-744 (May, 1997).									
an	AT	1	Long, J.R. and Copeland, M.A., *The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's,* IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, IEEE, pp. 357-369 (March, 1997).									
EXAMINER	\mathcal{M}	 /S	I			DATE CONSID	ERED 5/	16/5				
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INITIAL		DOCUMENT NUMBER			DATE	NAME	CLASS		SUB-CLASS	FILING DATE		
9	AA2	5,4	46,311		08/1995	Ewen et al.	*					
8	AB2	5,4	83,207	<u>'</u>	01/1996	Gabara						
2	AC2	+	25,325		04/1997	Rotzoll et al.	↓ =					
	AD2	† 	30,214		05/1997	Yamamoto et al.						
2	AE2		48,744		07/1997	Prakash et al.	1-4					
6	AF2	5,6	86,864	<u> </u>	11/1997	Martin et al.	 -					
8	AG2	5,7	15,012	2	02/1998	Patel et al.	\downarrow		- '			
2	AH2	5,7	17,243	3	02/1998	Lowther	\bot					
82L	Al2	5,7	37,035	5	04/1998	Rotzoil	3					
10m	AJ2	5,7	39,587	7	04/1998	Sato	┶					
97	AK2	5,8	25,600)	10/1998	Watt	-					
					FOREIC	ON PATENT DOCUMENTS						
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8	AL2	0	0 629 040 A1		12/1994	EP	H03D		1/22	Yes No		
	AM2	0	0 780 853 A1		06/1997	EP	H01F		17/00	Yes No		
0	AN2	2	2 058 505 A		04/1981	GB	Н	03D	7/12	Yes No		
0	A02	6	62-154607		07/1987	JP	H01F		15/04	Yes X No		
v	AP2	V	NO 97	/09786 A1	03/1997	РСТ	Н	03L	7/08	Yeş No		
					OTHER (Including A	uthor, Title, Date, Pertinent Pages, etc.)						
84	AR	2	Poole, S.J. et al., "A CMOS Subscriber Line Audio Processing Circuit Including Adaptive Balance," <i>IEEE International Symposium on Circuits and Systems Proceedings</i> , Vol. 2 of 3, IEEE, pp. 1931-1934 (1988).									
D	AS	2		Yue, C.P. and Wong, S.S., *On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's,* IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, IEEE, pp. 743-752 (May, 1998).								
en	АТ	2		English-language Abstract of Japanese Patent Publication No. 62-154607, 2 pages (July 9, 1987) - Date of Publication of Application).								
EXAMINER		N	N	15			T	DATE CON	SIDERED			
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				U.S.	PATENT DOCUMENTS						
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2	AA3	-	5,828,589	10/1998	Degenhardt	+					
9	AB3	_	5,150,891	11/2000	Welland et al.				i		
5	AC3	_	5,177,964 B1		Birleson et al.	\top					
6	AD3	_	5,426,680 B1	 	Duncan et el.						
	AE3	T									
	AF3	T									
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				FOREIG	ON PATENT DOCUMENTS						
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3	AL3		WO 98/50956 A1	11/1998	PCT	н	101L	29/00	Yes No		
	ЕМА								Yes No		
	AN3								Yes No		
	AO3	_				\perp		<u> </u>	Yes No		
	AP3	\bot							Yes No		
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